AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 11. (Canceled)

12. (New) An integrated circuit comprising:

a plurality of functional modules;

a bus comprising a crossbar switch interconnecting each of said plurality of functional modules; and

a common buffer disposed on said bus to store transfer information transferred from at least one source module to at least one destination module among said plurality of functional modules, wherein said common buffer is set in a buffering enabled state or a buffering disabled state dependent on whether or not a buffer in said destination module can accept said transfer information; and

means for selecting a path for transferring said transfer information to said destination module when a signal from said destination module indicates that said buffer within said destination module can accept said transfer information, and selecting a transfer path for storing said transfer information in said common buffer when the signal indicates that the buffer within said destination module cannot accept said transfer information,

wherein said common buffer on said bus is disposed in a vicinity of each of said plurality of functional modules.

13. (New) An integrated circuit according to claim 12, further comprising a signal line to transfer said transfer information to the buffer within said destination module when said buffer can accept said transfer information, said signal line circumventing said common buffer.

14. (New) An integrated circuit according to claim 12, wherein said destination module comprises an information receiving buffer to receive information from said common buffer, and

wherein, when said information receiving buffer cannot accept said transfer information, information indicating that no transfer can be permitted is communicated from said destination module to said source module.

15. (New) An integrated circuit comprising:

a bus comprising a crossbar switch interconnecting each of a plurality of functional modules, wherein said bus transmits transfer information from a source module to a destination module among said plurality of functional modules;

a controlling unit to select a transfer path depending on whether or not a buffer in said destination module can accept said transfer information;

a common buffer to store said transfer information transferred between said plurality of functional modules in accordance with the result of a selection made by said controlling unit when said buffer on said destination module cannot accept said transfer information; and

transfer path controlling means, including a plurality of common bus interfaces, for controlling input/output between said plurality of functional modules and said common buffers.

16. (New) An integrated circuit comprising:

a CPU module;

a first bus connected to an external memory interface module;

a second bus connected to a plurality of functional modules; and

a bus adapter to connect between said first bus and said second bus,

wherein said first bus comprises a crossbar switch interconnecting each of said CPU module, said external interface module, said plurality of functional modules and said bus adapter, and

wherein said integrated circuit further comprises:

a control unit to select a transferring path for transferring transfer information from a source module to a destination module in any of said CPU module, said external interface module, and said functional modules depending on whether said destination module can accept said transfer information;

a common buffer to store said transfer information depending on a result selected by said control unit when a buffer in said destination module cannot accept said transfer information; and

transfer path control means, comprising a plurality of common bus interfaces, for controlling input or output between said plurality of functional modules and said buffer.

17. (New) An integrated circuit according to claim 16, wherein said first bus employs a protocol identical to a protocol employed by said second bus.

18. (New) An integrated circuit according to claim 17, wherein an operating frequency of said first bus is an integer multiple of an operating frequency of said second bus.

19. (New) An integrated circuit according to claim 12, wherein said crossbar switch comprising said common buffer is disposed on a position facing to each of said plurality of functional modules and is connected thereto.

20. (New) An integrated circuit according to claim 12, wherein said crossbar switch comprising said common buffer is disposed on a nearest position to each of said plurality of modules and is connected thereto.

21. (New) An integrated circuit according to claim 12, wherein said crossbar switch comprising said common buffer is disposed in a neighborhood of a central portion of said integrated circuit and is connected thereto.

22. (New) An integrated circuit according to claim 12, wherein said crossbar switch comprises a plurality of selectors, and wherein each signal inputted from each of said plurality of modules is connected to said common buffer via said selector comprising said crossbar switch.

23. (New) An integrated circuit according to claim 22, wherein each signal outputted from said common buffer is outputted to each of said plurality of modules via an another selector comprising said crossbar switch.

24. (New) An integrated circuit according to claim 12, wherein said crossbar switch comprises:

a first crossbar switch unit to select any one of each of signals outputted from each of said plurality of modules;

a second crossbar switch unit to select either one a signal outputted from said common buffer or a signal outputted from said crossbar switch unit; and

a third crossbar switch unit to select an output destination of said plurality of modules.

AMENDMENTS TO THE DRAWINGS

The attached sheets of drawing include changes to Figs. 8 and 9 to replace the original sheets showing Figs. 8 and 9. These Figs. 8 and 9 have been labeled as prior art in response to the requirement to do so in the first paragraph in the Office Action.